DESIGN FOR RELIABILITY APPROACH FOR ELECTRONICS UNDER EXTREME LOW TEMPERATURE APPLICATIONS

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ABSTRACT

We present a design for reliability approach for electronics under low temperature applications. The proposed approach does not require altering the semiconductor processes and is focused on device parametric characterization, failure criteria determination, device and circuit/system reliability correlation, as well as reliability extrapolation.

1. INTRODUCTION

Electronics in space applications are often required to operate in low temperature environments, such as in any *in-situ* exploration missions to Mars, Titan, Europa and Lunar surfaces. In this paper, we present a design for reliability (DFR) approach for electronics under extreme low temperature applications. This approach is a paradigm shift from current reliability assessment for low temperature electronics and it provides the design fundamentals to build electronics for low temperature applications.

In the area of low temperature electronics, the majority of the research activities have been concentrated on the performance evaluation of the electronics; very few focus on the long term reliability issue. Our approach is targeting to ensure the required electronics lifetime under extreme low temperature environments, which is a critical requirement for mission success.

The fundamental reliability challenges for electronics operating under extreme low temperatures come from a specific failure mechanism called hot carrier aging (HCA) effect or any mechanisms related to and/or triggered by ion impact ionization process from device physics point of view [1-6]. Because of this physics failure phenomenon, an electronic device designed with a 10-year hot carrier aging lifetime under a temperature range of 27°C to 125°C has a much decreased lifetime at low temperatures, such as -230°C for lunar surface exploration.

Our approach does not require altering the process and so is a cost-efficient way to design for reliability under low temperature applications.

2. DESIGN FOR RELIABILITY APPROACH

It consists of the following aspects:

1) Evaluate hot carrier aging evaluation across the entire operating temperature range. The parametric degradation, including drain saturation and linear currents, threshold voltage, transconductance and drain conductance, needs to be fully characterized to evaluate the hot carrier aging impact on circuit/system.

2) Determine appropriate device hot carrier aging failure criteria to translate the hot carrier aging lifetime into circuit/system lifetime. Device parametric failure criteria need to be established to reflect the critical circuit performance requirements of circuit/system.

3) Project hot carrier aging lifetime from testing conditions to operating condition. A hot carrier aging lifetime projection/extrapolation model has been proposed to take into account both the device bias configuration and operating temperature profile.

4). Establish design guidelines to design for reliability. The most applicable transistor sizes are determined in order to meet reliability requirements.

3. CASE STUDY

Future surface exploration missions to Mars, Moon, Europa, Titan, etc. can expose spacecrafts or probes to a local extreme environments with temperatures as low as –230°C and temperature ranges as wide as wide –130°C to +90°C. The traditional solution in extreme environments has been to keep the electronics operating in a limited temperature range by housing them in a “warm-electronics-box” (WEB); however, this is not

viable for next-generation robotics and rovers, where electronics are placed at the point of use or next to loads directly exposed to the environment.

The case study assumes for a Mars mission using 0.6-µm commercial CMOS semiconductor technology with 5.0 V nominal V_{dd} and a 5-year lifetime on its critical path under a temperature range of –120°C to +80°C.

3.1 HCA evaluation

Hot carrier aging (HCA) tests were performed on the 0.6-µm NMOS transistors at room temperature (RT), –100ºC, and –150ºC. At –100ºC and –150ºC, the bias conditions include V_{ds} = 6.5 V, 6.0 V and 5.5 V, with V_{gs} = 2.0 V, 2.2 V, 2.4 V, 3.5 V, and 5.0 V to cover both maximum and non-maximum I_{sub} conditions.

During hot carrier aging tests, the parametric characteristics, i.e. saturation current I_{dsat}, linear current I_{dlin}, threshold voltage V_{th}, transconductance g_m, and drain conductance g_{ds}, were extracted from the I_{ds} versus V_{ds} and V_{gs} curves. Fig. 1 shows the maximum transconductance shift during the hot carrier aging at room temperature and -150ºC, as an example of parametric shifting observed during the hot carrier testing.

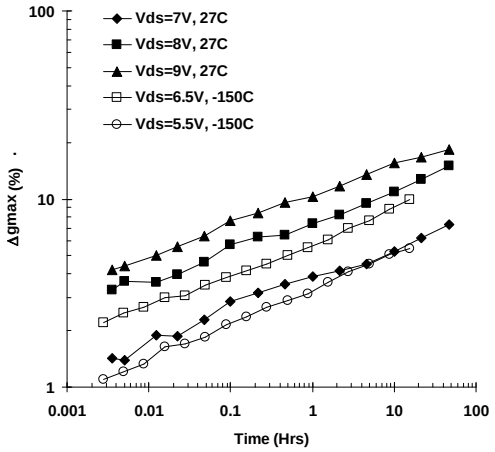

Fig. 1. g_{max} shift during hot carrier aging at room temperature and -150ºC.

3.2 Failure criterion determination

It has been demonstrated that the degradation of drain saturation current I_{dsat}, i.e., ΔI_{dsat} / I_{dsat} tracks and correlates with ring oscillator frequency degradation and a 10% I_{dsat} degradation typically yields a 5% frequency degradation [7-9]. Since drain saturation current I_{dsat} degradation on the NMOS transistors was found to be saturating around 2% to 5% both at room temperature and low temperatures, the digital circuitry does not appear to be the limiting factor for the low temperature circuit reliability.

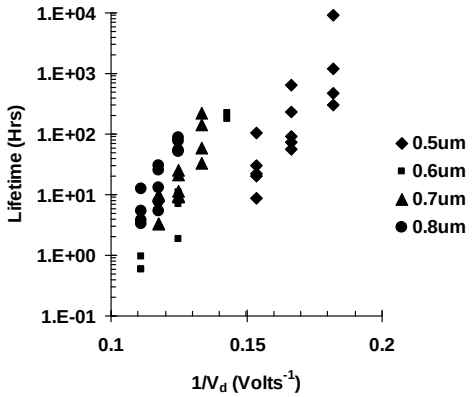

Fig. 2. Hot carrier aging tests at room temperature for NMOS transistors with different channel lengths.

For digital applications, the current drivability is the most significant device parameter, which can be described by I_{dsat}. In analog applications, the differential amplifier is one of the fundamental analog circuit building blocks; gain and offset voltage are the two most important performance parameters for the differential amplifier. The differential parameters transconductance g_m and drain conductance g_{ds} are essential, since the small-signal voltage gain, g_m/g_{ds}, is the maximum achievable single device amplification.

In the case of small-signal gain, a 75% small-signal gain corresponds to 15% maximum transconductance g_{max} change during the hot carrier aging [10]. Therefore, 15% g_{max} degradation was chosen as the failure criterion for the hot carrier aging lifetime for small-signal gain parametric.

In the case of offset voltage, 20 mV offset voltage was set as a failure criterion. This is equivalent to a 2% threshold change since the threshold voltage is approximately 1V. The relationship between the degradation of threshold voltage to that of maximum transconductance g_{max} indicated that a 2% threshold change was equivalent to a 10% maximum transconductance g_{max} change during the hot carrier aging [10]. Hence, 10% g_{max} degradation was chosen as the failure criterion for the hot carrier aging lifetime for fulfilling the offset voltage requirements.

3.3 Lifetime projection

Generally, worst-case hot carrier analysis has been used during process and technology qualification as well as product qualification [11]. This worst-case analysis usually only considers the N-channel metal-oxide semiconductor (NMOS) transistor hot carrier aging lifetime estimated under worst-case condition, i.e., maximum substrate current and minimum operating temperature. However, the worst-case hot carrier aging analysis approach typically gives a very conservative or, in some cases, an overly pessimistic prediction of NMOS lifetime. Therefore, a new methodology is desired and required to ensure the long-term reliability of electronics in low-temperature ranges.

Instead of using the worst-case analysis approach, which basically depends on the lowest temperature and maximum substrate current, we propose a new hot carrier aging lifetime extrapolation model that includes the temperature dependence of both substrate current and the hot carrier aging lifetimes. The extrapolation then becomes a function of transistor size and for the circuitry of interest, the target reliability requirement can be designed in by choosing the applicable transistor sizes along the critical paths. Please note that the applicable transistor size may not be the minimum channel length since, in some cases, transistors with longer channel length may have bias conditions which can generate more degradation due to hot carrier aging.

Assume 1) the degradation resulting from hot carrier aging is cumulative; 2) there is negligible annealing effect at higher temperatures, the input information to be determined is I_{sub} temperature dependence, I_{sub} profile, and operation temperature profile.

Substrate current is temperature dependent and since hot carrier aging lifetime is a function of substrate current, substrate-current temperature dependence is one of the most important factors needed, and is normally determined from experiments.

Typically, the expected hot carrier aging lifetime t_{50} is a function of substrate current I_{sub}.

Significant substrate current, and hot carrier aging, is present only during voltage transition. I_{sub} is not a constant value but changes over time. During each voltage transition, I_{sub} versus time is defined as an I_{sub} profile and can be determined by circuit simulation and/or experiments. Each I_{sub} profile can be divided into j small time intervals, where a constant substrate current I_{sub} is assumed during each time interval t_j.

During each time interval t_j, the NMOS transistor experiences a stress condition characterized by I_{sub}, and has a corresponding life time expectation of t_{50}, however, the transistor is biased under this I_{sub} only for a period of t_j. Therefore, the percentage of the NMOS transistor lifetime consumed during the time interval t_j is defined as $p(t_i)$ and can be then expressed as

$$p(t_i) = \frac{t_i}{t_{50}(I_{sub})} \tag{1}$$

t_{50} is the expected device hot carrier aging lifetime under the I_{sub} during the time interval t_j. The percentage of the device hot carrier aging lifetime consumed during one I_{sub} cycle is then $p(I_{sub})$ and is given by

$$p(I_{sub}) = \sum_{m=1}^{j} \frac{t_m}{t_{50}(I_{sub,m})} \tag{2}$$

The operating temperature profile shows the expected temperature changes over time under use conditions. The profile can be the temperature change over a day, a month, a year, or any time span.

Similar to the I_{sub} profile, the operating-temperature profile is divided into k intervals, where each interval is one I_{sub} profile cycle, assuming the I_{sub} cycle is typically very small since I_{sub} is a function of temperature**.** Again, a constant temperature can be assumed for each I_{sub} cycle and the percentage of the device hot carrier aging lifetime consumed during one operating temperature profile is $p(T)$, shown as follows:

$$p(T) = \sum_{n=1}^{k} \sum_{m=1}^{j} \frac{t_{m,n}}{t_{50}(I_{sub,m}, T_n)} \tag{3}$$

Assume the operating temperature profile is the temperature changes over a day and the reliability requirement of a circuit is D days; then the percentage of device hot carrier aging lifetime taken during D days is $p(D)$, given by:

$$p(D) = D * (\sum_{n=1}^{k} \sum_{m=1}^{j} \frac{t_{m,n}}{t_{50}(I_{sub,m}, T_n)}) \tag{4}$$

By setting (5) equal to one, we can determine the number days, given by (6), that the device can survive from the hot carrier aging point of view. Therefore, the minimum NMOS transistor channel length to satisfy the following expression with any desirable margin is:

$$D > (1/\sum_{n=1}^{k}\sum_{m=1}^{j}\frac{t_{m,n}}{t_{50}(I_{sub,m},T_n)}) \qquad (5)$$

3.4 Design guidelines

Based on substrate current profile, temperature profile and channel length dependence, Fig. 3 gives the air temperature profile on Mars and Fig. 4 shows the projected hot carrier aging lifetime as a function of channel length under the Mars temperature profile.

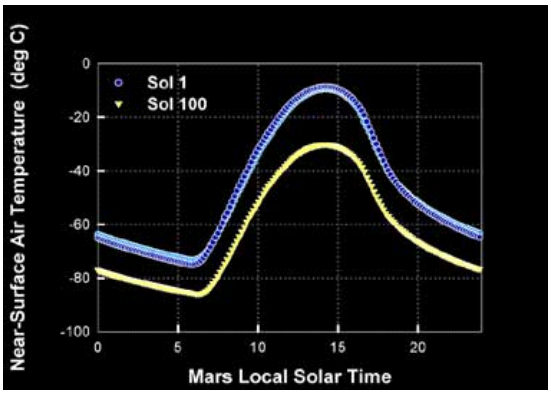

Fig. 3 Air temperature profile on Mars.

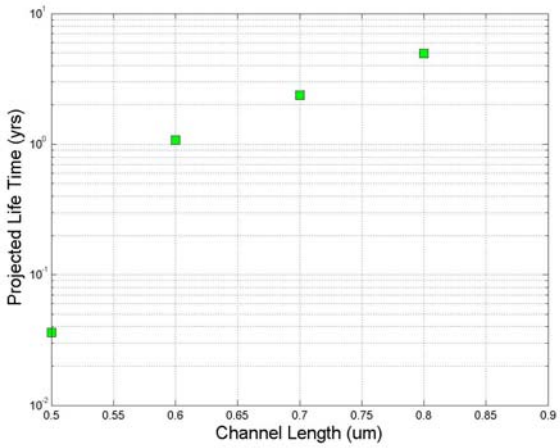

Fig. 4. An example of the projected NMOS hot carrier aging lifetime under a Mars temperature profile.

4. SUMMARY

A design for reliability approach for electronics under low temperature applications, which does not require altering the semiconductor processes, is presented. A case study has been used to demonstrate the approach on device parametric characterization, failure criteria determination, device and circuit/system reliability correlation, as well as reliability extrapolation.

5. ACKNOWLEDGEMENT

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